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10/720,611	11/24/2003	Chih-Ching Lin	10113281	4244

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,611	LIN ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 25 is objected to because of the following informalities: In line 2 of claim 25, "12" should be changed to "21", otherwise claim 25 is identical to claim 16. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Since to form a bit line contact the dielectric layer is etched while the barrier spacer remains in place, it is desirous to use an etch with a high selectivity of the dielectric relative to the barrier spacer, not the opposite, as claimed. For the purposes of determining patentability, the claim will be treated as best interpreted by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21, 22, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu (U.S. 6,037,228).

Regarding claim 21, Hsu teaches a method of forming bit line contact comprising the steps of providing a substrate having a plurality of transistors therein (Fig. 2C), each comprising a gate electrode (**204** in Fig. 2C) and doping areas serving as drain and source (**218** in Fig. 2C; column 3, lines 54-56); forming a pair of barrier spacers on the opposite sidewalls between gate electrodes (**216** in Fig. 2C); forming a dielectric layer on the surface of the gate electrodes, barrier spacers and doping areas; and using the barrier spacer and the substrate as an etch stop, etching a portion of the dielectric layer to form a bit-line contact (column 3, lines 57-64).

Regarding claim 22, Hsu teaches the method of forming a bit line contact as claimed in claim 21, wherein the barrier spacer comprises materials having semiconducting properties (polysilicon, column 3, lines 48-50).

Regarding claim 24, Hsu teaches the method of forming a bit line contact as claimed in claim 21, wherein the dielectric layer comprises oxygen-containing silicate (silicon oxide, **220** in Fig. 2D; column 3, lines 57-58).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chung et al. (U.S. 6,787,415).

Regarding claim 1, Hsu teaches a method of forming bit line contact comprising the steps of providing a substrate having a plurality of transistors therein (Fig. 2C), each comprising a gate electrode (**204** in Fig. 2C) and doping areas serving as drain and source (**218** in Fig. 2C; column 3, lines 54-56); forming a polysilicon spacer on the sidewalls of the gate electrodes (**216** in Fig. 2C; column 3, lines 48-50); forming a dielectric layer overlying the surface of the gate electrodes, polysilicon spacers and doping areas; and using the polysilicon spacer and the substrate as an etch stop, etching a portion of the dielectric layer to form a bit line contact (column 3, lines 57-64).

Hsu does not teach forming a mask layer to cover a portion of the polysilicon spacer, and removing the unmasked portion of the polysilicon spacer, and removing the mask layer.

Chung et al. teaches forming a mask layer to cover a portion of a polysilicon spacer, and removing the unmasked portion of the polysilicon spacer (Fig.3A; column 5, lines 27-31), and removing the mask (subsequent processing step, dopant implantation, would not be performed with the mask layer in place).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hsu and Chung et al. by forming a bit line contact as taught by Hsu, and removing a portion of the polysilicon spacer, as taught by Chung et al., before forming a dielectric layer. The motivation for doing so at the time of the invention would have been because the portion of the spacer etched off was not necessary for the device to function, as taught by Chung et al. (column 5, line 27).

Regarding claim 2, together Hsu and Chung et al. teach the method of forming a bit line contact as claimed in claim 1. Chung et al. further teaches that the formation of the polysilicon spacer on the sidewalls of the gate electrode further comprises forming a conformal polysilicon layer on the surface of the gate electrodes and doping areas (column 5, lines 7-16; and anisotropically etching the polysilicon layer, such that the remaining polysilicon layer forms a polysilicon spacer on the sidewalls of the gate electrodes (column 5, lines 20-26).

Regarding claims 3 and 4, together Hsu and Chung et al. teach the method of forming a bit line contact as claimed in claim 2. Chung et al. further teaches that the polysilicon layer is formed by low pressure chemical vapor deposition (LPCVD) (column 5, lines 7-9) and that the polysilicon spacer is etched using reactive ion etching (RIE) (column 5, lines 20-22).

Regarding claim 5, together Hsu and Chung et al. teach the method of forming a bit line contact as claimed in claim 1. Hsu further teaches that the dielectric layer comprises an oxygen-containing silicate (silicon oxide, column 3, lines 56-57).

Regarding claim 7, together Hsu and Chung et al. teach the method of forming a bit line contact as claimed in claim 1. Hsu teaches that the gate electrode comprises a cap layer on the top of the gate electrode (**206a** in Fig. 2B), and an oxide spacer on the sidewalls of the gate electrode (**212** in Fig. 2B). Hsu does not teach that the spacer on the sidewalls of the gate electrode is made of silicon nitride.

Chung et al. teaches that the gate electrode comprises a cap layer on the top of the gate electrode (**290** in Fig. 3A), and a silicon nitride spacer on the sidewalls of the gate electrode (**170** in Fig. 3A; column 5, lines 1-3).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a bit line contact according to the method claimed in claim 1, as taught by Hsu and Chung et al. together, and further form a silicon nitride spacer on the sidewalls of the gate electrode, as taught by Chung et al. The motivation for doing so at the time of the invention would have been to insert an intervening layer with a low etch selectivity relative to polysilicon to act as an etch stop between the polysilicon spacer and the gate electrode to protect the gate electrode from the subsequent etch of the unmasked polysilicon spacers (Chung et al., column 5, lines 27-31), and to separate the gate electrode, **140** in Fig. 7, from the polysilicon spacer, **160** in Fig. 3A (column 3, lines 12-15).

Regarding claim 26, Hsu teaches the method of forming a bit line contact as claimed in claim 21 (note 35 U.S.C. 102(b) rejection above), wherein the gate electrode comprises a cap layer on the top of the gate electrode (**206a** in Fig. 2B), and an oxide spacer on the sidewalls of the gate electrode (**212** in Fig. 2B). Hsu does not teach that the spacer on the sidewalls of the gate electrode is made of silicon nitride.

Chung et al. teaches forming a silicon nitride spacer on the sidewalls of the gate electrode (**170** in Fig. 3A; column 5, lines 1-3) to separate the gate electrode, **140** in Fig. 7, from the polysilicon spacer, **160** in Fig. 3A (column 3, lines 12-15).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a bit line contact according to the method taught by claim 21 and by Hsu and further form a silicon nitride spacer on the sidewalls of the gate electrode, as taught by Chung et al. The motivation for doing so at the time of the invention would have been to separate the gate electrode from the polysilicon spacer, as expressly taught by Chung et al., and additionally to protect the gate electrode from the subsequent etch of the polysilicon spacers (Chung et al., column 5, lines 27-31).

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chung et al. (U.S. 6,787,415) as applied to claim 1 above, and further in view of Chan et al. (U.S. 6,383,921).

Regarding claims 9 and 10, together Hsu and Chung et al. teach the method of forming a bit line contact as claimed in claim 1 (note 35 U.S.C. 103(a) rejection above). They do not teach before forming the dielectric layer, forming a liner layer on the surface of the gate electrodes, polysilicon spacers, and doping areas, wherein the liner layer is silicon nitride.

Chan et al. teaches a method of forming a contact comprising forming a liner layer (**116** in Fig. 3) made of silicon nitride on the surface of a gate electrode, polysilicon spacers, and doping areas (Fig. 3), before forming a dielectric layer, in order to protect the area where a contact is not to be formed (column 3, lines 17-29).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a bit line contact using the method of claim 1 as taught by Hsu and Chung et al. together and further form a silicon nitride liner layer on the surface

of the gate electrodes, polysilicon spacers, and doping areas before forming the dielectric layer, as taught by Chan et al. The motivation for doing so at the time of the invention would have been to protect the area where a contact is not to be formed, as noted above as taught by Chan et al.

Claims 12-15, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chung et al. (U.S. 6,787,415) and Chan et al. (U.S. 6,383,921).

Regarding claim 12, Hsu teaches a method of forming bit line contact comprising the steps of providing a substrate having a plurality of transistors therein (Fig. 2C), each comprising a gate electrode (**204** in Fig. 2C) and doping areas serving as drain and source (**218** in Fig. 2C; column 3, lines 54-56); forming a conformal polysilicon layer on the surface of the gate electrodes and doping areas; etching the polysilicon layer, such that the polysilicon layer forms a polysilicon spacer on the sidewalls of the gate electrodes (column 3, lines 48-50; Fig. 2C); forming a dielectric layer on the surface of the gate electrodes, the polysilicon spacers, and the doping areas; and using a polysilicon spacer and the substrate as an etch stop, etching a portion of the dielectric layer to form a bit line contact (column 3, lines 57-64); and filling a conductive layer into the bit line contact as a bit line contact plug (**224** in Fig. 2D; column 4, lines 7-9).

Hsu does not teach forming a mask layer on the surface of the gate electrode doping area and a portion of the gate electrode located on both sides of the doping area; and removing the unmasked portion of the polysilicon spacer by etching; removing the mask layer and forming a liner layer overlying the surface of the gate electrodes, the

polysilicon spacers and the doping areas; forming a dielectric layer on the liner layer; and etching a portion of the liner layer.

Chung et al. teaches forming a mask layer on the surface of the gate electrode doping area and a portion of the gate electrode located on both sides of the doping area; and removing the unmasked portion of the polysilicon spacer by etching, and removing the mask layer (Figs. 3A, 7; column 5, lines 27-31; subsequent processing step, dopant implantation, would not be performed with the mask layer in place).

Chan et al. teaches forming a liner layer (**116** in Fig. 3) overlying the surface of the gate electrodes, the polysilicon spacers and the doping areas; forming a dielectric layer on the liner layer (column 3, lines 30-32); and etching a portion of the liner layer (column 3, lines 33-37).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a bit line contact using the method taught by Hsu, and additionally form a mask layer on the surface of the gate electrode doping area and a portion of the electrode located on both sides of the doping area, remove the unmasked portion of the polysilicon spacer by etching, and remove the mask, as taught by Chung et al. The motivation for doing so at the time of the invention would have been because the portion of the spacer etched off was not necessary for the device to function, as taught by Chung et al. (column 5, line 27). Additionally, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a liner layer overlying the surface of the gate electrodes, the polysilicon spacers, and the doping areas, to protect the area where a contact is not to be formed, as taught by Chan et al. (column 3,

lines 17-29). In order to use the polysilicon spacer as an etch stop, the etching the portion of the dielectric layer to form a bit line contact, as taught by Hsu, would necessarily entail etching a portion of the liner layer, as taught by Chan et al., which would arrive at the invention as specified in claim 12.

Regarding claims 13 and 14, together Hsu, Chung et al., and Chan et al. teach the method of forming a bit line contact as claimed in claim 12. Chung et al. further teaches that the polysilicon layer is formed by low pressure chemical vapor deposition (LPCVD) (column 5, lines 7-9) and that the polysilicon spacer is etched using reactive ion etching (RIE) (column 5, lines 20-22).

Regarding claim 15, together Hsu, Chung et al., and Chan et al. teach the method of forming a bit line contact as claimed in claim 12. Hsu further teaches that the dielectric layer comprises an oxygen-containing silicate (silicon oxide, column 3, lines 56-57).

Regarding claim 17, together Hsu, Chung et al., and Chan et al. teach the method of forming a bit line contact as claimed in claim 12. Chung et al. further teaches that the gate electrode comprises a cap layer on the top of the gate electrode (**290** in Fig. 3A), and a silicon nitride spacer on the sidewalls of the gate electrode (**170** in Fig. 3A; column 5, lines 1-3).

Regarding claim 19, together Hsu, Chung et al., and Chan et al. teach the method of forming a bit line contact as claimed in claim 12. Chan et al. further teaches that the liner layer is silicon nitride (column 3, lines 26-28).

Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chan et al. (U.S. 6,383,921).

Regarding claims 27 and 28, Hsu teaches the method of forming a bit line contact as claimed in claim 21 (note 35 U.S.C. 102(b) rejection above), but does not teach before forming the dielectric layer, forming a liner layer on the surface of the gate electrodes, barrier spacers, and doping areas, wherein the liner layer is silicon nitride.

Chan et al. teaches a method of forming a contact comprising forming a liner layer (**116** in Fig. 3) made of silicon nitride on the surface of a gate electrode, polysilicon spacers, and doping areas (Fig. 3), before forming a dielectric layer, in order to protect the area where a contact is not to be formed (column 3, lines 17-29).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a bit line contact using the method of claim 1 as taught by Hsu and further form a silicon nitride liner layer on the surface of the gate electrodes, polysilicon spacers, and doping areas before forming the dielectric layer, as taught by Chan et al. The motivation for doing so at the time of the invention would have been to protect the area where a contact is not to be formed, as noted above as taught by Chan et al.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chung et al. (U.S. 6,787,415) as applied to claim 1 above, and further in view of Wolf et al. (S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era*, Vol. 1).

Together Hsu and Chung et al. teach the method of forming a bit line contact as claimed in claim 1 (note 35 U.S.C. 103(a) rejection above), wherein the dielectric layer is formed using chemical vapor deposition, but not specifically LPCVD, PECVD, HDPCVD, APCVD, or SACVD.

Wolf et al. teaches that dielectrics such as silicon dioxide can be formed at low temperatures via APCVD (pg. 190, second paragraph), which results in lower-density dielectric layers than thermal SiO_2.

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to form a bit line contact according to the method of claim 1 and taught by Hsu and Chung et al. together, and form the dielectric layer via APCVD, as taught by Wolf et al. The motivation for doing so at the time of the invention would have been to achieve a low-density dielectric layer, as expressly taught by Wolf (pg. 190, paragraph 4).

Claims 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chung et al. (U.S. 6,787,415) and Chan et al. (U.S. 6,383,921) as applied to claim 12 above, and further in view of Wolf et al. (S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era*, Vol. 1).

Regarding claim 16, Together Hsu and Chung et al. and Chan et al. teach the method of forming a bit line contact as claimed in claim 12 (note 35 U.S.C. 103(a) rejection above), wherein the dielectric layer is formed using chemical vapor deposition, but not specifically LPCVD, PECVD, HDPCVD, APCVD, or SACVD.

Wolf et al. teaches that dielectrics such as silicon dioxide can be formed at low temperatures via APCVD (pg. 190, second paragraph), which results in lower-density dielectric layers than thermal SiO_2.

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to form a bit line contact according to the method of claim 1 and taught by Hsu and Chung et al. and Chan et al. together, and form the dielectric layer via APCVD, as taught by Wolf et al. The motivation for doing so at the time of the invention would have been to achieve a low-density dielectric layer, as expressly taught by Wolf (pg. 190, paragraph 4).

Regarding claim 20, together Hsu, Chung et al., and Chan et al. teach the method of forming a bit line contact as claimed in claim 12, but do not teach that the dielectric layer and liner layer are etched using MERIE, ECR, or RIE.

Wolf et al. teaches that it is favorable to use MERIE to etch dielectrics including SiO_2 because they offer satisfactory etching performance for many dielectric etching applications required in deep-submicron fabrication processes, and is a lower-cost alternative to high-density plasma etchers (pg. 703, lines 1-5).

Therefore, at the time of the invention, it would have been obvious to form a bit line contact as claimed in claim 12, and as taught by Hsu, Chung et al., and Chan et al. together, by etching the dielectric using MERIE, as taught by Wolf et al. The motivation for doing so at the time of the invention would have been because MERIE is a lower-cost alternative to high-density plasma etching, as expressly taught by Wolf et al.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chung et al. (U.S. 6,787,415) as applied to claim 1 above, and further in view of Chan et al. (U.S. 6,383,921), as applied to claim 9 above, and further in view of Wolf et al. (S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era*, Vol. 1).

Regarding claim 11, together Hsu, Chung et al., and Chan et al. teach the method of forming a bit line contact as claimed in claim 9, but do not teach that the dielectric layer and liner layer are etched using MERIE, ECR, or RIE.

Wolf et al. teaches that it is favorable to use MERIE to etch dielectrics including SiO_2 because they offer satisfactory etching performance for many dielectric etching applications required in deep-submicron fabrication processes, and is a lower-cost alternative to high-density plasma etchers (pg. 703, lines 1-5).

Therefore, at the time of the invention, it would have been obvious to form a bit line contact as claimed in claim 9, and as taught by Hsu, Chung et al., and Chan et al. together, by etching the dielectric using MERIE, as taught by Wolf et al. The motivation for doing so at the time of the invention would have been because MERIE is a lower-cost alternative to high-density plasma etching, as expressly taught by Wolf et al.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Wolf et al. (S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era*, Vol. 1).

Hsu teaches the method of claim 21 (note 35 U.S.C. 102(b) rejection above), wherein the wherein the dielectric layer is formed using chemical vapor deposition, but not specifically LPCVD, PECVD, HDPCVD, APCVD, or SACVD.

Wolf et al. teaches that dielectrics such as silicon dioxide can be formed at low temperatures via APCVD (pg. 190, second paragraph), which results in lower-density dielectric layers than thermal SiO_2.

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to form a bit line contact according to the method of claim 21 and taught by Hsu, and form the dielectric layer via APCVD, as taught by Wolf et al. The motivation for doing so at the time of the invention would have been to achieve a low-density dielectric layer, as expressly taught by Wolf (pg. 190, paragraph 4).

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Ding et al. (U.S. 5,814,563).

Hsu teaches the method of forming a bit line contact as claimed in claim 21 (note 35 U.S.C. 102(b) rejection above), but does not teach that during the etching of the portion of the dielectric layer, the etching selectivity of the barrier spacer to the dielectric layer exceeds 50:1.

Ding et al. teaches a method of etching silicon oxide with an etch selectivity relative to polysilicon that exceeds 50:1 (column 12, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hsu and Ding et al. by forming a bit line contact according to the method of 21, as taught by Hsu, wherein while etching the

portion of the silicon oxide dielectric layer, the etching selectivity of the dielectric layer to the polysilicon spacer exceeds 50:1. The motivation for doing so at the time of the invention would have been because the etching system taught by Ding et al. offers a large process window for processing semiconductor substrates in a range of different process conditions without significantly reducing the silicon oxide etch rate, as expressly taught by Ding et al. (column 12, lines 40-47). Additionally, the dielectric etch shown in Hsu's Fig. 2D requires a high etch selectivity of silicon oxide relative to polysilicon.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chung et al. (U.S. 6,787,415) as applied to claim 7 above, and further in view of Linliu et al. (U.S. 5,688,713).

Together Hsu and Chung et al. teach the method of forming a bit line contact as claimed in claim 7 (note 35 U.S.C. 103(a) rejection above), but they do not teach that during etching of the unmasked polysilicon spacer, the etching selectivity of the polysilicon spacer to the cap layer of the gate electrode exceeds 50:1.

Linliu et al. teaches a method of plasma etching polysilicon spacers using a silicon nitride layer as an etch stop. The plasma etch to remove the spacers is carried out using a high selective etch rate of polysilicon to silicon nitride (column 8, lines 27-41). It would be obvious to form a bit line contact according to the method claimed in claim 7, as taught by Hsu and Chung et al. together, wherein the cap layer of the gate electrode is silicon nitride, as taught by Hsu, and optimize the etching characteristics to obtain the highest etch selectivity possible, one that exceeds 50:1, between polysilicon and silicon nitride. It has been held that

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality .... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955).

The instant specification does not disclose the critical nature of an etch selectivity of the polysilicon spacer to the cap layer of the gate electrode that exceeds 50:1.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. 6,037,228) in view of Chung et al. (U.S. 6,787,415) and Chan et al. (U.S. 6,383,921) as applied to claim 17 above, and further in view of Linliu et al. (U.S. 5,688,713).

Together Hsu and Chung et al. and Chan teach the method of forming a bit line contact as claimed in claim 7 (note 35 U.S.C. 103(a) rejection above), but they do not teach that during etching of the unmasked polysilicon spacer, the etching selectivity of the polysilicon spacer to the cap layer of the gate electrode exceeds 50:1.

Linliu et al. teaches a method of plasma etching polysilicon spacers using a silicon nitride layer as an etch stop. The plasma etch to remove the spacers is carried out using a high selective etch rate of polysilicon to silicon nitride (column 8, lines 27-41). It would be obvious to form a bit line contact according to the method claimed in claim 7, as taught by Hsu and Chung et al. and Chan together, wherein the cap layer of

the gate electrode is silicon nitride, as taught by Hsu, and optimize the etching characteristics to obtain the highest etch selectivity possible, one that exceeds 50:1, between polysilicon and silicon nitride. It has been held that

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality .... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955).

The instant specification does not disclose the critical nature of an etch selectivity of the polysilicon spacer to the cap layer of the gate electrode that exceeds 50:1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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ERIK KIELIN
PRIMARY EXAMINER

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